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New PMOS LTPS–TFT pixel for AMOLED to suppress the hysteresis effect on OLED current by employing a reset voltage driving

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Abstract

New PMOS LTPS (low temperature polycrystalline silicon)–thin film transistor (TFT) pixel circuit, which can suppress an OLED current error caused by the hysteresis of LTPS–TFT for active matrix organic light emitting diode (AMOLED) display, is proposed and fabricated. The proposed pixel circuit employs a reset voltage driving so that the sweep direction of gate voltage in the current driving TFT is not altered by the gate voltage in the previous frame. Our experimental results show that OLED current error of the proposed pixel is successfully suppressed because a reset voltage can enable the starting gate voltage for a desired one not to be varied, while that of the conventional 2-TFT pixel exceeds over 15% due to the hysteresis of LTPS–TFT.

Keywords: Hysteresis; AMOLED; TFT pixel

1. Introduction

Recently, organic light emitting diode has gained much attention due to its compactness, wide-viewing angle [1]. Active matrix OLED (AMOLED), which employs thin film transistor (TFT) pixels, has been attracted for a low power consumption and high resolution display [2]. Therefore, a stable thin film is studied for a display application [3]. Recently, poly-Si TFTs are attractive pixel elements for AMOLED due to their superior current-stability [2,4]. However, they suffer from a current non-uniformity due to fluctuation of excimer laser energy. In addition to the current non-uniformity, hysteresis phenomenon is also observed in the poly-Si TFTs. One possibility of the cause of the hysteresis effect is an interface trap density between Si layer and oxide layer. Residual image due to the hysteresis phenomenon of poly-Si TFT, such that the previous display image remains apparent in the subsequent image, may be another problem observed in conventional poly-Si TFT pixel composed of 2-TFT [5]. Although the current-uniformity of poly-Si TFT will be improved by the process development, the hysteresis phenomenon is existed due to an interface trap density. Therefore, the hysteresis phenomenon should be resolved by the process development or circuit approach. Most of the previous works to suppress the hysteresis of TFT are the device approach, such as a plasma treatment on the interface [6]. We have recently reported a-Si:H TFT pixel, which can suppress the hysteresis effect on I_{OLED} by resetting a gate voltage of the current driving TFT [7].

The purpose of our work is to report poly-Si pixel driving scheme to suppress the hysteresis effect on I_{OLED}. Our experimental results show that under the proposed pixel driving scheme, I_{OLED} variation caused by the hysteresis can successfully be eliminated due to the fixed V_{GS} sweep direction of poly-Si TFT.

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2. Analysis of hysteresis in poly-Si TFT

In order to investigate the hysteresis phenomenon of poly-Si TFT, we have fabricated PMOS-poly-Si TFT, which is usually used in the AMOLED display, at a low temperature of less than 450 °C on a 1737 Corning glass substrate. The standard commercial PMOS process for a top-gate TFT is employed in this experiment [4].

Fig. 1(a) shows the measured hysteresis phenomenon of poly-Si TFT, and Fig. 1(b) is the magnified data of Fig. 1(a). Fig. 1(b) shows the hysteresis effect on the drain current of poly-Si TFT. When a desired gate-source voltage is applied from both high current and low current, the drain current can be varied with a gate-voltage sweep direction, such as reverse or forward direction. Reverse gate-voltage sweep is from $V_{GS} = -20$ V to 15 V, whereas forward is from $V_{GS} = 15$ V to -20 V, respectively. The sweep speed was 12 V/s.

In order to investigate the cause of the hysteresis phenomenon, we measured the transfer characteristics in the forward-voltage sweeps with different starting gate voltages, such as 0 V and 30 V, as shown in Fig. 2. The sweep speed was also 12 V/s. By employing different starting gate voltages, different quantities of charge were trapped at the interface so that the transfer curve is shifted with a different starting voltage.

The shift in transfer curves caused by hysteresis phenomenon would be attributed to differences in quantities of charge trapped at the interface, as shown in Fig. 3. As the starting gate voltage became much positive (30 V), an electron in the poly-Si channel layer is much formed and trapped to the interface trap density, which is a fast states. Trapped electron can reduce threshold voltage of PMOS–TFT due to the screening effect of gate voltage on the TFT. Hysteresis phenomenon can be also explained by the charge balance equation. The charge balance equation can be expressed as $(Q_G + Q_I + Q_S) = 0$, where Q_G is the gate charge, Q_I is an insulator charge, and Q_S is the silicon charge. Q_I includes the interface trap charges between silicon and insulator layer, so that $Q_I = Q_f + Q_{it}$, where Q_f represents fixed insulator charges and Q_{it} represents interface charges. Fixed oxide charges are located in the deep states of the insulator; thus, these do not relate with the hysteresis, which is a short-time effect. The Q_{it} contribution to Q_I is the cause of the hysteresis phenomenon. The

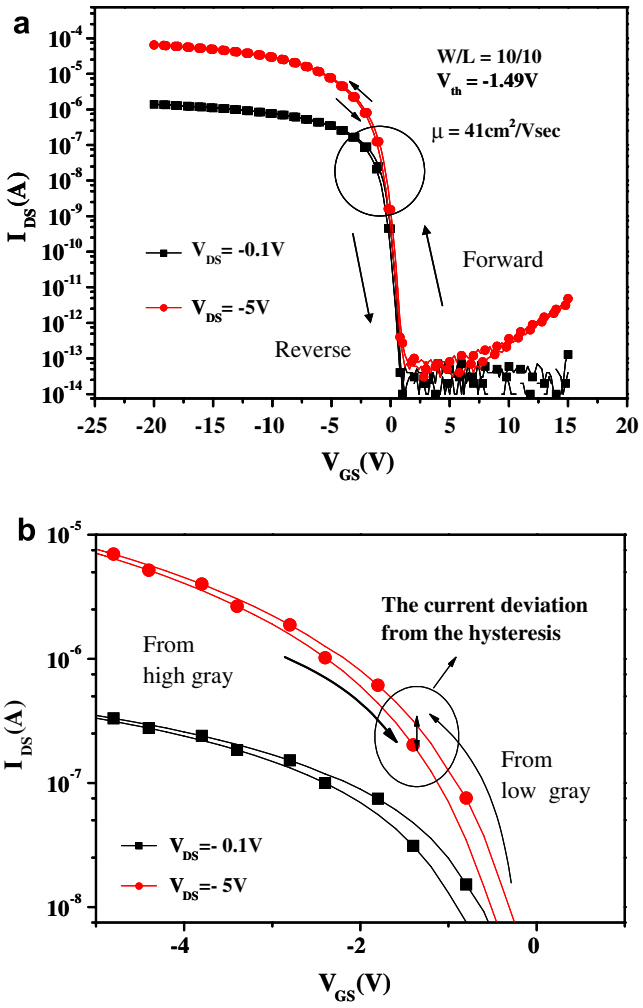

Fig. 1. (a) Transfer characteristics of PMOS–TFT. (b) Magnified data showing a hysteresis effect on the drain current of poly-Si TFT. The sweep speed was 12 V/s.

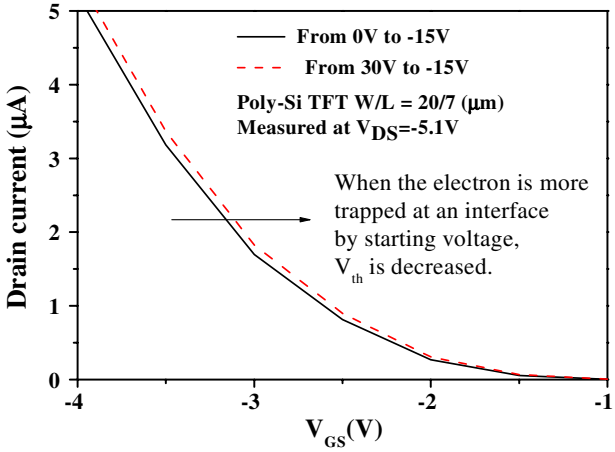

Fig. 2. The transfer characteristics in the forward-voltage sweeps with different starting gate voltages. The sweep speed was 12 V/s.

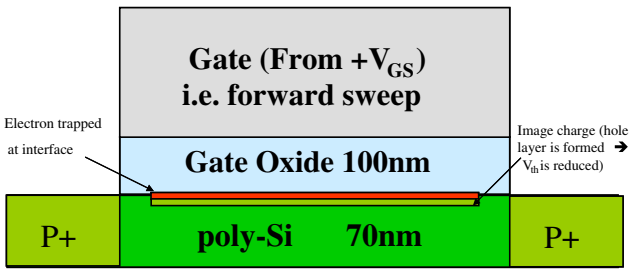

Fig. 3. The interface trapped charge by starting gate voltage, resulting in the threshold voltage variation of poly-Si TFT.

mobile charge drift is influenced by temperature and bias duration. Temperatures up to 150 °C with long bias duration are high enough to ensure that the available sodium ions drift completely across the oxide. However, we made measurements at room temperature and for a short period (several sec), so that the mobile charge drift might not occur. Thus, we can conclude that the Q_{it} (interface trapped charges) contribution to Q_i is the cause of hysteresis phenomena. In Fig. 2, for a larger starting gate voltage (30 V) in the PMOS–TFT, an extra $\Delta Q_G > 0$ is required, due to the positive shift of the transfer curve. Under the same drain current, an increased gate charge ($\Delta Q_G > 0$) is the result of a decrease in effective interface charges ($\Delta Q_{it} < 0$) between silicon and insulator layer because Q_S is constant; for a more positive starting gate voltage in the forward voltage sweeps of PMOS–TFT. A decrease in effective interface charges ($\Delta Q_{it} < 0$) is consistent with an electron trapped at the interface due to the positive starting gate voltages.

In order to investigate the relation between an observed hysteresis and OLED current error, we have measured a current with different starting gate-voltage in the poly-Si TFT device. Fig. 4 is the output current variation in the device with a different starting gate-voltage, from −3 V to −7 V. The gate node of current driving TFT in the well known 2-TFT pixel circuit experiences a very fast data voltage transition during one row time (∼several 10 μs). Thus, we measured the drain current at only two gate-source voltages (for example from $V_{GS} = 0$ V to 4 V or $V_{GS} = 8$ V to 4 V) with fixed drain voltage ($V_{DS} = -5$ V). We changed the gate source voltage within 640 μs. Our experimental results in Fig. 4 shows that the same gate-source ($V_{GS} = -5$ V) and drain-source ($V_{DS} = -5$ V) voltages exhibits the different output current with the previous gate-source voltage due to hysteresis phenomenon with a different starting gate-voltage. For example, the drain current of 8.4 μA was measured at a previous gate-source voltage of $V_{GS} = -3$ V, whereas that of 7.7 μA was measured at a previous gate-source voltage of $V_{GS} = -5$ V, and that of 7.45 μA was measured at a previous gate-source voltage of $V_{GS} = -7$ V, respectively.

3. Suppressing hysteresis effect on the pixel

When an identical V_{GS} and V_{DS} are applied to poly-Si TFT, the drain current of TFT is varied due to the hysteresis phenomenon, which makes the variation of drain current according to a gate-voltage (V_{GS}) sweep direction. In order to suppress the hysteresis effect on I_{OLED}, we propose that a reset voltage should be applied before a data of a present frame is written, which enables V_{GS} sweep direction of current-driving TFT to be fixed.

Fig. 5 shows the proposed poly-Si TFT pixel driving scheme, which can apply a reset voltage before a data voltage is applied to a pixel, to eliminate I_{OLED} variation due to the hysteresis of poly-Si TFT. When the proposed driving scheme is employed in the panel, only one TFT (T3) and one clock signal line are required for one row line. Moreover it could be applied in the other driving pixel circuit which can compensate the current non uniformity of poly-Si TFT. The operation of the proposed reset voltage-driven pixel is as follows. When a clock signal is a low state (reset voltage), T3 is turned on so that a gate node voltage of T2 would be discharged to a low voltage of clock signal (V_{LOW}) until T3 is turned off. Therefore, the gate voltage of T2 is discharged to $V_{LOW} + V_{TH\_T3}$. When a clock signal is higher than a data voltage, T3 is turned off due to $V_{GS\_T3} = 0$ so that T2 can supply I_{OLED} in accordance with a data voltage. Therefore, V_{GS} sweep direction of T2 is always forward direction, such as from $V_{LOW} + V_{TH\_T3}$ to the data voltage and the gate starting voltages of T2 are independent of the data voltages. When T3 threshold voltage is varied in the pixel to pixel, the starting gate voltage may be varied. However, the V_{th} variation of poly-Si TFT is known less than ±0.3 V. In this V_{th} variation (±0.3 V), the drain current variation induced by the hysteresis may not much affected. Though the V_{th} variation

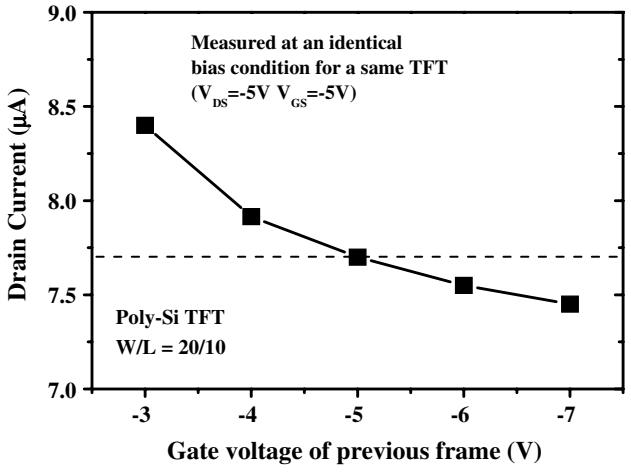

Fig. 4. The output current variation in the device with a different starting gate-voltage, from −3 V to −7 V.

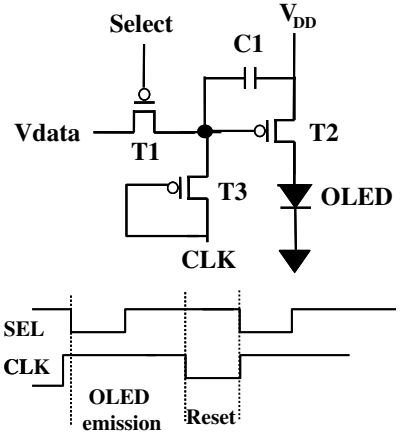

Fig. 5. The proposed reset voltage-driven pixel and a timing diagram.

of T3 induces a variation of starting gate voltages, the drain current may not be affected.

In order to verify the reset voltage driven proposed pixel, we have performed SPICE simulation for checking the gate voltage of T2. Fig. 6 shows SPICE simulation results, which can successfully reset the gate voltage of T2 before a data voltage is written. In this simulation, we can conclude that the proposed pixel can reset the gate voltage of T2.

Fig. 7 shows the photography of the fabricated pixel on a glass substrate by employing a standard commercial PMOS process. OLED current is evaluated by a well known diode connected TFT and parasitic capacitance. Detailed device parameters are as follows. Storage capacitor is 0.3 pF. The channel length of T1 and T2 is fixed to be 8 μm, whereas that of T3 is 40 μm for reducing a leakage current of T3. The channel width of T2 is designed to be 20 μm. The channel widths of T1 and T3 are 10 μm.

Fig. 8 shows I_{OLED} in the conventional and proposed pixel when I_{OLED} in the previous frame is varied in order to check the hysteresis effect on I_{OLED}. When we apply the data voltage of 8.5 V (mid-current) from both 7.5 V (high current, ~2 μA) and 8.5 V (low current, ~100 nA) to the conventional 2-TFT pixel, I_{OLED} is varied from 1096 nA to 930 nA due to the difference of previous data voltages, as shown in Fig. 8 (a). I_{OLED} variation due to the hysteresis is reduced with increasing an operation time due to its recoverable characteristics [3]. The desired current for 8 V data voltage (~1 μA) in the proposed pixel, from both 7.5 V (~2 μA) and 8.5 V (~0.1 μA), is not varied. The desired I_{OLED} of the proposed pixel is independent of the I_{OLED} of previous frame due to a fixed V_{GS} sweep direction, while that of the conventional pixel is dependent on the previous I_{OLED} due to the hysteresis of poly-Si TFT causing a drain current variation according to V_{GS} sweep direction.

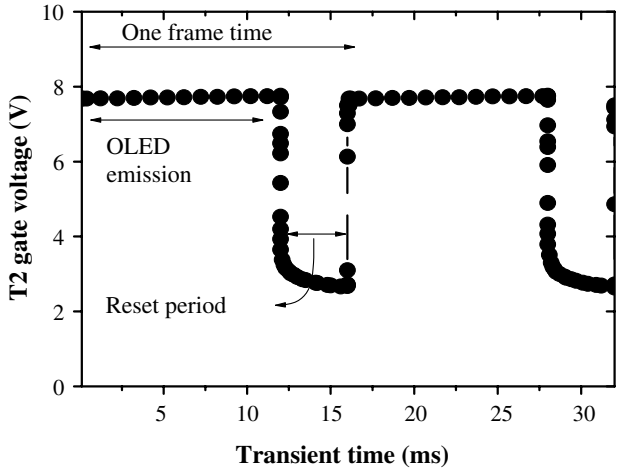

Fig. 6. SPICE simulation results, which can successfully reset the gate voltage of T2 before a data voltage is written.

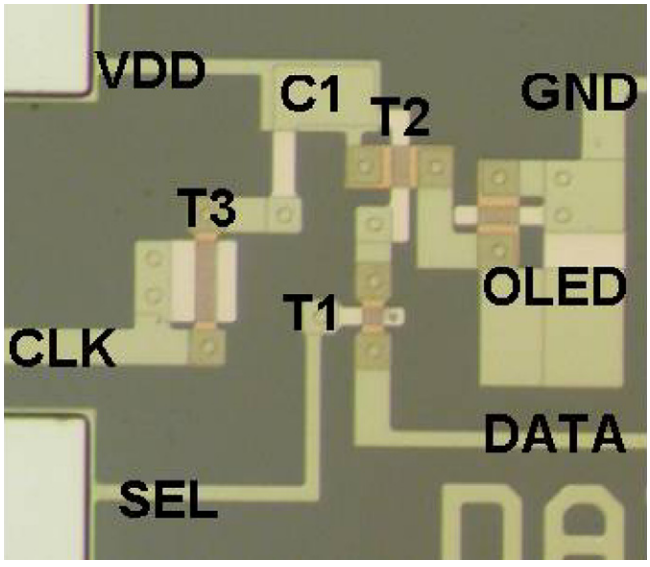

Fig. 7. The photography of the fabricated pixel on a glass substrate.

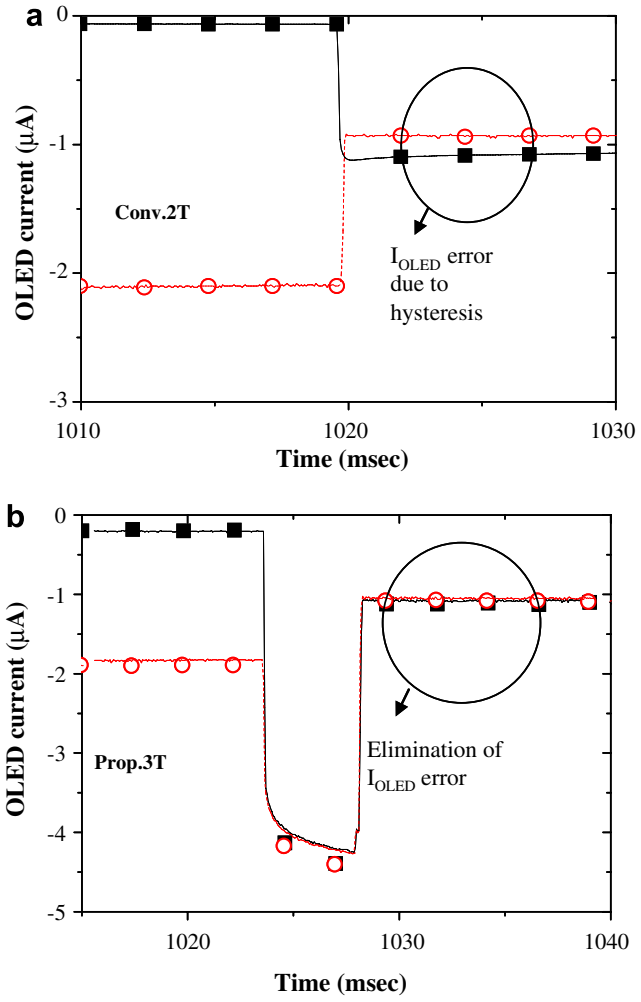

Fig. 8. (a) I_{OLED} in the conventional and (b) that in the proposed pixel.

4. Summary

We have proposed and fabricated new LTPS-TFT AMOLED pixel circuit, which considerably suppresses an OLED current error caused by the hysteresis of LTPS–TFT by employing a reset voltage driving. Our experimental results show that OLED current error of the proposed pixel is successfully suppressed because a reset voltage can enable the starting gate voltage for a desired one not to be varied, while that of the conventional 2-TFT pixel exceeds over 10% due to the hysteresis of LTPS–TFT.

The proposed poly-Si TFT pixel may be suitable to suppress the hysteresis effect on OLED current for a high quality AMOLED display.

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